THE CLAIMS

1. A magnetic memory cell comprising first and second magneto-resistive devices connected in series, the first magneto-resistive device having a first sense layer, the second magneto-resistive device having a second sense layer, the first and second sense layers having different coercivities.

2. The memory cell of claim 1, wherein the first and second devices are magnetic tunnel junctions.

3. The memory cell of claim 2, wherein the first magnetic tunnel junction includes the first sense layer and a first pinned layer; and wherein the second magnetic tunnel junction includes the second sense layer and a second pinned layer.

4. The memory cell of claim 2, wherein the sense layers of the first and second devices are back to back; and wherein the sense layers are separated by a layer of non-magnetic material.

5. The memory cell of claim 2, wherein the first and second magnetic tunnel junctions share a pinned layer.

6. The memory cell of claim 2, wherein hysteresis loops of the first and second junctions are nested.

7. The memory cell of claim 1, wherein the sense layers in the first and second devices have different shapes.

8. The memory cell of claim 1, wherein the sense layers in the first and second devices have different sizes.

9. The memory cell of claim 1, wherein the sense layers of the first and second devices have different shapes and sizes.

10. The memory cell of claim 1, wherein the sense layers of the first and second devices have different thicknesses.

11. The memory cell of claim 1, wherein the sense layers of the first and second devices are made of different materials.

12. The memory device of claim 1, wherein the first and second devices have distinguishably different delta resistances, whereby the memory cell has at least four distinguishable logic states.

13. An information storage device comprising:

an array of memory cells; and

a plurality of first and second traces for the array, the first and second traces extending in different directions;

each memory cell being at a cross point of a first trace and a second trace;

at least some of the memory cells including series-connected first and second magnetic tunnel junctions, sense layers of the first and second junctions having different coercivities.

14. The information storage device of 13, wherein each first magnetic tunnel junction includes a first sense layer and a first pinned layer; and wherein each second magnetic tunnel junction includes a second sense layer and a second pinned layer.

15. The information storage device of claim 13, wherein the sense layers of the series-connected junctions are connected in series; and wherein the series-connected sense layers are separated by a layer of non-magnetic material.

16. The information storage device of claim 13, wherein the series-connected magnetic tunnel junctions have shared pinned layers.

17. The information storage device of claim 13, wherein hysteresis loops of series-connected junctions are nested.

18. The information storage device of claim 13, wherein the sense layers in the series-connected first and second junctions have different shapes.

19. The information storage device of claim 13, wherein the sense layers in the series-connected first and second junctions have different sizes.

20. The information storage device of claim 13, wherein the sense layers of the series-connected first and second junctions have different thicknesses.

21. The information storage device of claim 13, wherein the sense layers of the series-connected first and second junctions are made of different materials.

22. The information storage device of claim 13, wherein the series-connected first and second junctions have distinguishably different delta resistances, whereby each memory cell having series-connected junctions has at least four distinguishable logic states.

23. A method of fabricating a magnetic memory device, the method comprising:

forming a first stack of magnetic memory layers on a substrate, the first stack including a first sense layer;

forming a second stack of magnetic memory layers on the first stack, the second stack including a second sense layer;

the first and second sense layers being made to have different coercivities.

24. The method of claim 23, wherein the second stack is deposited on the first stacks; the first and second stacks are patterned into bits having a first shape; and at least the sense layer of the second stack is re-patterned into a different second shape.

25. The method of claim 23, wherein the sense layers of the first and second stacks are made with at least one of different size, shape and material.